29.4 Hierarchical Power Distribution with 20 Power Domains in 90-nm Low-Power Multi-CPU Processor

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A power gating scheme with several power-domain partitions is commonly used to reduce leakage current in low-power SoCs [1, 2]. However, the number of CPUs and/or DSPs integrated on a single SoC is increasing and the leakage current is ever increasing. Fine-grained power gating using dozens of power domains, like fine-grained clock gating for decreasing switching power, is becoming indispensable. To achieve this, we have developed a hierarchical power distribution (HPD) with a power tree, which is analogous to the structure of clock tree, and demonstrates dozens of power domain integrations in a 90-nm one-chip 3G cellular phone processor.

The conventional partitioning shown in Fig. 29.4.1 has one or two constantly powered domains and three or four power domains, with each domain powered on and off depending on the operational mode [1, 2]. Conventional partitioning has a star structure, which makes it difficult to increase the number of power domains over more than a dozen, where as HPD has a tree structure and incorporates dozens of power domains. The three power-tree management rules shown in Fig. 29.4.2 and the common power domain (CPD) shown in Fig. 29.4.3 are the keys to overcoming the following three major issues with partitioning dozens of power domains. These issues are a long global signal transmission between two distant power domains (e.g. clock buffers and repeaters), an invalid signal transmission from the power-off domain to the power-on one, and a long recovery time from the power-off state to the power-on state caused by the restoration of lost data in the powered-off state.

An isolation cell, which we call µI/O [3], is commonly used to prevent the invalid signal transmission from the power-off domain. The power-tree management rules shown in Fig. 29.4.2 minimize the number of isolation cell insertions and make logic verification easy. The top level of the power distribution hierarchy is a permanently powered-on domain that is used for I/Os. Rule 1 is that domains on lower levels of the hierarchy (e.g. PDx) can be in the powered-on state only if the domains on the higher levels of the hierarchy (e.g. PDy) are on. Rule 2 is that the isolation cell is placed in a higher level of the hierarchy (e.g. PDy) when a signal is transmitted from a lower level (e.g. PDx) to a higher one (e.g. PDy) in the hierarchy. Rule 3 is that a signal can transit on the graph of power tree.

The CPD prevents the long global signal transmission and reduces the long recovery time with minimal area overhead. As shown in Fig. 29.4.3, the CPD is distributed over the entire SoC. As an example of a long global signal transmission, global clock buffers can be placed in the distributed CPD, while local clock buffers are placed in each power domain. Therefore, having dozens of power-domain partitions does not increase the clock skew. In addition, backup latches are placed in the CPD near the original FFs. Key information (e.g. the states of the control register, the clock, and the interrupt settings) for achieving a quicker recovery is stored in the backup latches before the domain enters a power-off state and then it is restored to the original FFs during a recovery operation.

Figure 29.4.4 shows the power switch (PSW) configurations for the power domains, the CPD, and the SRAM. There are three global power lines: VDD, VSS, and VSSM_CPD. The VSSM_CPD is the power-gated ground line for the CPD. The power lines are laid out horizontally across the chip. Local power lines for each power domain (VSSM_PDx) are also laid out horizontally on the same layer, but dedicated to each power domain. The power switches for each power domain are placed vertically across the chip on the two opposite sides of each power domain. Those for the CPD are placed along the two sides of the chip vertically. The SRAM has its own embedded dedicated power switches for achieving the low-leakage retention mode [4].

The power switch consists of a thick-gate-oxide high-Vth NMOS, which is used for I/O circuitry. The 3.3V I/O supply (VCC) is applied to the gate of the power switches to provide sufficient on-resistance, even under a low-voltage supply for core circuitry (VDD). In 90nm processes, the gate-tunneling current is not negligible. It constitutes about 10% of the total leakage at room temperature. However, the power switch more than sufficiently suppresses both the sub-threshold and gate-tunneling currents. The leakage reduction ratio was about 1/4000 for a power domain with one million gates.

Turning on the power switches may cause a large rush current on the power line. Figure 29.4.5 shows the power switch controller (PSWC). A fast transition time between the power-off and on states, without a rush current, was achieved by using a newly developed precise gate-voltage sensing scheme in combination with a low-slew-rate driving scheme [3]. This sensing scheme detects a 90% drive of the gate of the power switches to the VCC voltage using a dynamic comparator. It effectively reduces the time margin. A dynamic comparator was used to make the process migration easy, to lower the PSWC's standby current, and to minimize the area overhead. A power domain with one million gates had a 3.9µs recovery time and a 53.8mA rush current under worst rush-current conditions.

Figure 29.4.6 depicts a 90nm application processor for a 3G cellular phone [1], which has a single CPU and several dedicated IPs for multimedia applications, with a conventional power domain design (on the left) and a 90nm one-chip 3G cellular phone processor [5], which has two CPUs, a baseband processor, and several dedicated IPs, with a hierarchical power distribution (on the right). The latter chip was implemented to partition a single SoC into 20 power domains, and a few on-chip voltage monitors (VMONs) were implemented in several of the power domains to measure the power supply drop due to the rush current. A mV drop in voltage was successfully measured by the VMONs, which converted the local supply voltage fluctuation into a frequency-modulated oscillation, and is presented as an external chip output. Figure 29.4.7 shows the measured voltage drop with the one-chip 3G cellular phone processor and that under the worst-load case in TEG. It revealed that the voltage drop was small under the worst case and was negligible under actual operations.

References:

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[4] M. Yamaoka, et al., "Low-Power Embedded SRAM Modules with Expanded Margins for Writing," *ISSCC Dig. Tech. Papers*, pp. 480-481, Feb., 2005.

[5] T. Hattori, et al., "A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor," *ISSCC Dig. Tech. Papers*, Paper 29.5, Feb., 2006.

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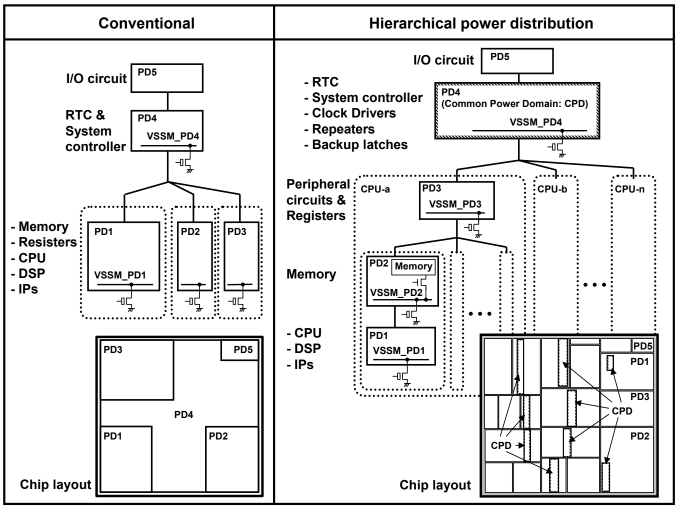

Figure 29.4.1: Partitioning dozens of power domains using hierarchical power distribution with power tree.

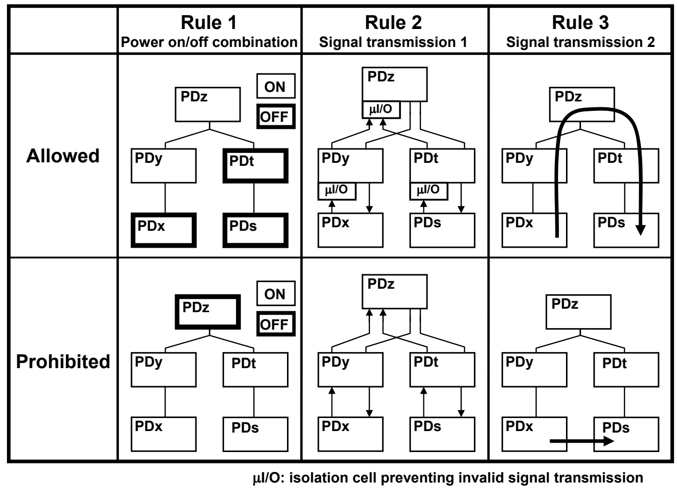

Figure 29.4.2: Three power-tree management rules.

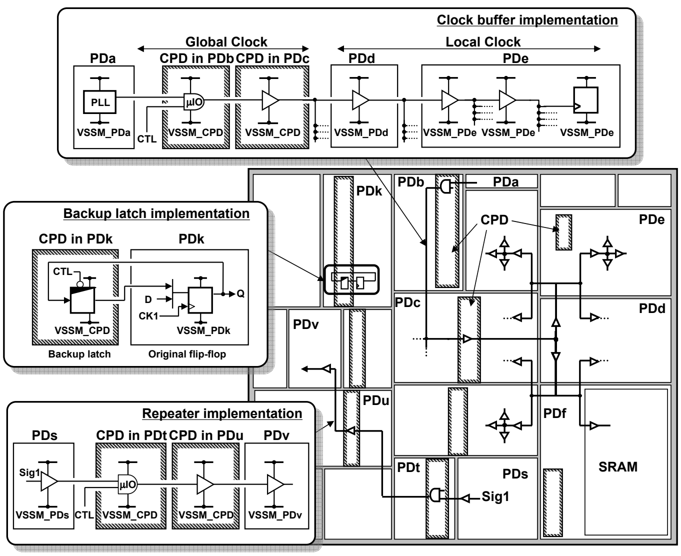

Figure 29.4.3: Common power domain (CPD) implementation.

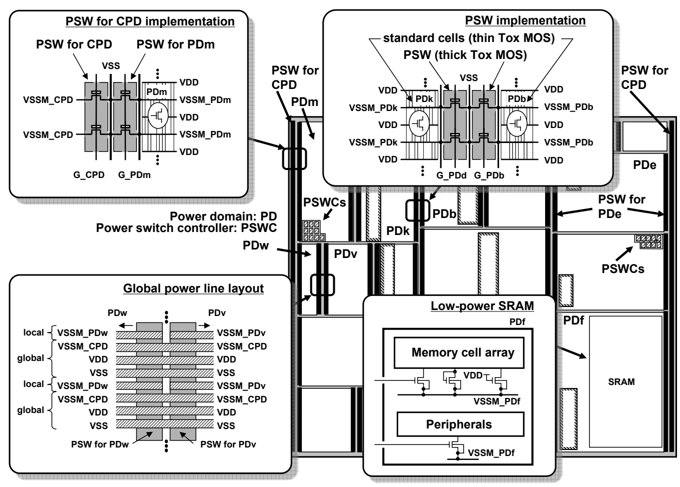

Figure 29.4.4: Power switch (PSW) configuration.

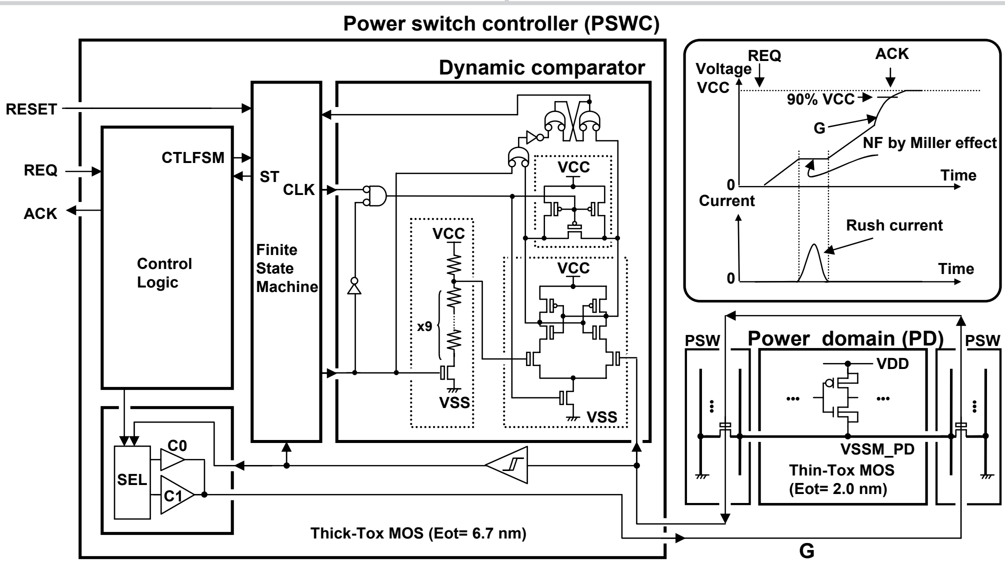

Figure 29.4.5: Power switch controller with dynamic comparator.

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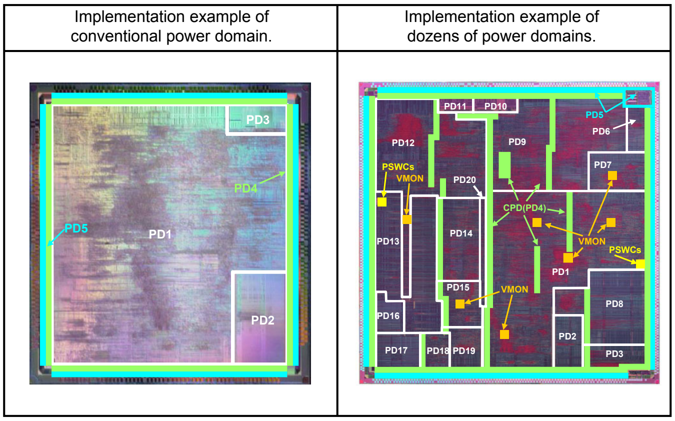

Figure 29.4.6: Micrographs of power domains.

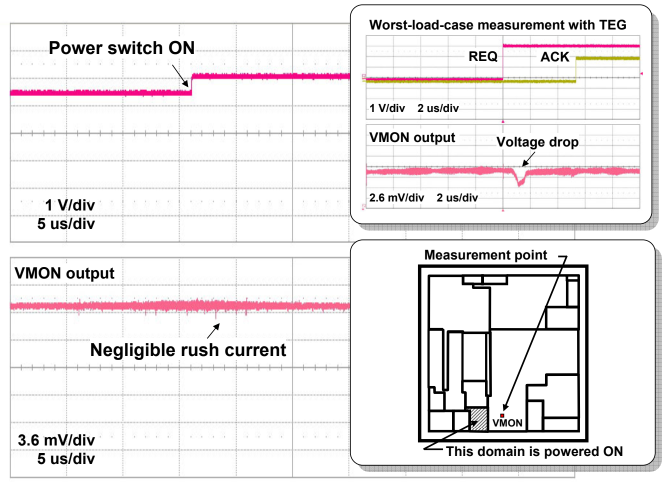

Figure 29.4.7: Measured waveforms of voltage monitor (VMON).